# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

1                                    **REMARKS**

2   These remarks follow the order of the paragraphs of the office action. Relevant portions of the

3   office action are shown indented and italicized.

4                                    *Claim Objections*

5      *1.      Claims 9, 18, 19 and 20 are objected to because of the following informalities:*

6      *applicant applies short-hand drafting to make claims appear dependent, but the*

7      *aforementioned claims are clearly independent claims as indicated by their distinct*

8      *preambles. Applicant's Deposit Account #: 09-0468 will be charged $600.00 for an additional*

9      *three independent claims (there are three independent claims in excess of three) as per 37*

10     *CFR 1.16(h) as authorized in the 07/15/2003 transmitted letter.*

11  Applicants respectfully states that since charges are already accrued claims 9, 18, 19 and 20 are

12  amended to be independent claims. This overcomes the objections to claims 9, 18, 19 and 20 .

13                                 *Claim Rejections - 35 USC § 102*

14     *2.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that*

15     *form the basis for the rejections under this section made in this Office action:*

16     *A person shall be entitled to a patent unless   (b) the invention was patented or described in a printed publication in this or a*

17     *foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the*

18     *United States.*

19     *3.      Claims 1-20 rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,448,702 to*

20     *Garcia, Jr, et al. (hereafter Garcia)*

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PAGE 7/13 * RCVD AT 8/4/2005 11:49:03 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/31 * DNIS:2738300 * CSID:9149453281 * DURATION (mm-ss):04-08

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1  Applicants respectfully states that the present invention provides apparatus for controlling flow

2  of data between first and second data processing systems via a memory, the apparatus comprising

3  descriptor logic for generating a plurality of descriptors including a frame descriptor defining a

4  data packet to be communicated between a location in the memory and the second data

5  processing system, and a pointer descriptor identifying the location in the memory; and a

6  descriptor table for storing the descriptors generated by the descriptor logic for access by the first

7  and second data processing systems. The descriptor logic and descriptor table improve efficiency

8  of data flow control between the first and second data processing systems such as a host

9  computer system and a data communications interface for communicating data between the host

10  computer system and a data communications network.


11  Garcia's invention is to provide a processor/adapter arrangement permitting a processor to

12  dispatch CDB's serially from noncontiguous locations in a memory, for defining a series of data

13  transfer operation to be conducted in a continuously active adapter channel, wherein the

14  dispatching functions of the processor can be discarded out without any coordination to activities

15  in the respective channel and wherein the adapter invariably will perform the operations defined

16  by the dispatched CDB's in a reliable manner, without compromising any activities in the

17  respective channel. In accordance with Garcia, "a computer system and DMA (direct memory

18  access) channel adapter are configured to co-operate in the formation and modification of linked

19  list queues of chained descriptors/Con's while an adapter channel to which the respective queue

20  is directed is active, and to carry out the queue formation/modification procedure in potentially

21  optimal time coordination with the adapter's handling of data transfers relative to the respective

22  channel and queue; whereby a COB can be added to or removed from a virtually empty queue

23  (i.e. a queue whose CDB's have all been processed by the adapter) with minimal overall impact

24  on processor and adapter performance."


25  Garcia apparently is only in regard to **storing** descriptors, not with **generating** descriptors as in

26  claim 1. Thus the present invention and that of Garcia are clearly different, even though some

27  same and/or similar words are used. Thus claims 1-20 are indeed allowable over Garcia.


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1     *4.     As per claims 1 and 10, Garcia discloses an apparatus and method (Fig. 9)*

2     *comprising: descriptor logic (Fig. 2-4 shown how descriptors are implemented, e.g., in*

3     *form a linked list and pointer; Fig. 5 shows the components of a descriptor), said*

4     *apparatus for controlling flow of data between first and second data processing systems*

5     *via a memory (Column 18, lines 53-65, the adaptor in Fig. 9 is connected to the processor*

6     *and memory which it assists in communications with DMA, the processor is in Fig. 1,*

7     *element 2 and memory is Fig. 1, element 3), said descriptor logic for generating a plurality*

8     *of descriptors including a frame descriptor defining a data packet to be communicated*

9     *(Frame descriptor is shown in Fig. 5, element 52-55, where it dictates where to point the*

10     *data to next and the amount of data in the packet) between a location in the memory and*

11     *the second data processing system (Column 4, line 62-Column 5, line 10, where the*

12     *apparatus in Fig. 5 transfers descriptors in memory to a plurality of peripheral devices,*

13     *e.g., other data processing systems), and a pointer descriptor identifying the location in*

14     *the memory (Fig. 5, element 52 or 54); and a descriptor table (Fig. 4) for storing the*

15     *descriptors generated by the descriptor logic for access by the first and second data*

16     *processing systems (contains a linked list of descriptors).*

17     Applicants respectfully state that Claim 1 reads:

18     1. An apparatus comprising:

19     descriptor logic, said apparatus for controlling flow of data between first and second data

20     processing systems via a memory, said descriptor logic for generating a plurality of

21     descriptors including a frame descriptor defining a data packet to be communicated

22     between a location in the memory and the second data processing system, and

23     a pointer descriptor identifying the location in the memory; and

24     a descriptor table for storing the descriptors generated by the descriptor logic for access

25     by the first and second data processing systems.

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1  Garcia is apparently not concerned with "controlling flow of data between first and second data

2  processing systems via a memory," of Claim 1. Garcia is concerned with "permitting a processor

3  to dispatch CDB's serially from noncontiguous locations in a memory, for defining a series of

4  data transfer operation to be conducted in a continuously active adapter channel," not with flow

5  control as in claim 1.

6  Garcia apparently does not refer to, and is not concerned with "generating a plurality of

7  descriptors," nor with "a frame descriptor," nor with "defining a data packet to be communicated

8  between a location in the memory and the second data processing system," nor with, "a pointer

9  descriptor identifying the location in the memory." The office action is apparently employing

10 hindsight regarding the elements in Garcia's Figures 2-5, to construct the elements of claim 1. It

11 is well established that hindsight may not be employed in rejecting a claim. Garcia apparently

12 makes no reference to, nor is concerned with the invention of claim 1.

13 In claim 1, the descriptor table is [from present specification page 5, lines 7-12] "for storing the

14 descriptors generated by the descriptor logic for access by the first and second data processing

15 systems. The descriptor logic and descriptor table improve efficiency of data flow control

16 between the first and second data processing systems such as a host computer system and a data

17 communications interface for communicating data between the host computer system and a data

18 communications network." Whereas Garcia provides, [col. 3, lines 29-33] "a processor/adapter

19 arrangement as above, in which the adapter contains registers, dedicated to the continuously active

20 channel associated with the dispatched series of CDB's, for holding a "Channel Descriptor Table" (CDT)

21 useful by the adapter for constructing a linked list queue defining the number of COB's in the dispatched

22 series, which have not yet been processed by the adapter, and defining the locations in memory of at

23 *least a* first and last unprocessed COB's In the series." Garcia 'Channel Descriptor Table' is indeed a

24 table, but it is not "a descriptor table for storing the descriptors generated by the descriptor logic,"

25 as in claim 1. Garcia apparently is only in regard to **storing** descriptors, not with **generating**

26 descriptors as in claim 1. Thus claim 1, and all claims that depend on claim 1, are allowable over

27 the cited art.

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1    These same remarks are relevant for the allowance of claims 9, 10, 18, 19 and 20, which arc

2    allowable over the cited art.


3    *5.       As per claims 2,3,11 and 12, Garcia discloses claims 1 and 10, wherein the*

4    *descriptor  table is stored in the data processing system (Fig. 3, stored in adaptor registers, Fig.*

5    *9).*


6    Applicants respectfully state that the office action is apparently unclear in regard to the rejection

7    of claims 2, 3, 11 and 12 [and then claims 1 and 10]. It is noted that the remarks regarding

8    apparatus claim 1, are similarly relevant for differentiating method claim 10 from Garcia. Thus

9    claim 10, and all claims that depend on claim 10, are allowable over the cited art. Thus all

10   claims are allowable over Garcia.


11   Apparently the elements of claims 1, 2, 3,  10, 11 and 12, are reconstructed by the office action

12   into items in  Garcia's Figs 3 and 9. The elements in claims 1, 2, 3,  10, 11 and 12 and the

13   descriptor table for descriptors generated [claims 1 and 10] have little if any relationship to those

14   in Garcia's figures. Thus, claims 1, 2, 3,  10, 11 and 12 are allowable over Garcia.


15   *6.       As per claims 4-6, 13 and 14, Garcia discloses claims 1 and 10, wherein the*

16   *descriptor  logic generates various branch descriptor comprising links to other*

17   *descriptors in the descriptor  table (Fig. 3, various descriptors shown branching/pointing*

18   *to the next descriptor).*


19   Applicants respectfully state that it was shown above that Garcia indeed does not disclose claim

20   1 or claim 10.  Garcia apparently does not generate any descriptors, nor refers to a cyclic

21   descriptor list.  The office action is apparently again employing hindsight regarding the elements

22   in Garcia's figures to  construct the elements of claims 4-6, 13 and 14. It is well established that

23   hindsight may not be employed in rejecting a claim. Thus Garcia indeed does not disclose the

24   elements of claims 4-6, 13 and 14, which are all allowable in themselves and because each

25   ultimately depends on an allowable claim.


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1        7.     *As per claims 7 and 15, Garcia discloses claims 1 and 10, wherein the first data*

2        *processing system comprises a host system (Fig. 1, the adapter, MAU is part of a host*

3        *processing system). .*

4   Applicants respectfully state that it was shown above that Garcia indeed does not disclose claim

5   1 or claim 10. There are indeed many patents that refer to a host system. Claims 7 and 15 are

6   used for claim differentiation, and are indeed allowable in themselves and because each depends

7   on an allowable claim.

8        8.     *As per claims 8 and 16, Garcia discloses claims 1 an 10, wherein the second data*

9        *processing system comprises a data communications interface for communicating data*

10       *between the host computer system and a data communication network (Column 9, lines*

11       *1-8, adaptors are attached external networks).*

12  Applicants respectfully state that it was shown above that Garcia indeed does not disclose claim

13  1 or claim 10. A review of Garcia shows that Garcia is apparently not concerned with "a data

14  communications interface for communicating data between the host computer system and a data

15  communications network," of claims 8 and 16. These are not the adaptors of Garcia even if the

16  adaptors may be attached external networks. Thus claims 8 and 16 are indeed allowable in

17  themselves and because each depends on an allowable claim.

18       9.     *As per claim 9, Garcia discloses a data processing system (Fig. 1) comprising a host*

19       *processing system having a memory (element 2), a data communications interface (Fig. 1,*

20       *element 4.5) for communicating data between the host computer system and a data*

21       *communication network (Column 9, lines 1-8).*

22  Applicants respectfully state that the office action is apparently again employing hindsight

23  regarding the elements in Garcia's figures to construct the elements of claim 9. It is well

24  established that hindsight may not be employed in rejecting a claim.

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1   *10.    As per claims 17-20, Garcia discloses a computer program product, article of*

2   *manufacture and program storage device readable by a machine (Fig. 1, shows computer*

3   *product the result of manufacture, where the processor inherently requires initial*

4   *instruction, e.g., booting and initialization, in order to start operation) in accordance to*

5   *claims 1, 9 and 10.*

6   It is anticipated that this amendment brings the application to allowance of claims 1-20, and

7   favorable action is respectfully solicited. In the event that any claim remains rejected, please call

8   the undersigned.

9   Please charge any fee necessary to enter this paper to deposit account 50-0510.

10                                                                 Respectfully submitted,

11                                            By:    _____

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